

FIG 1

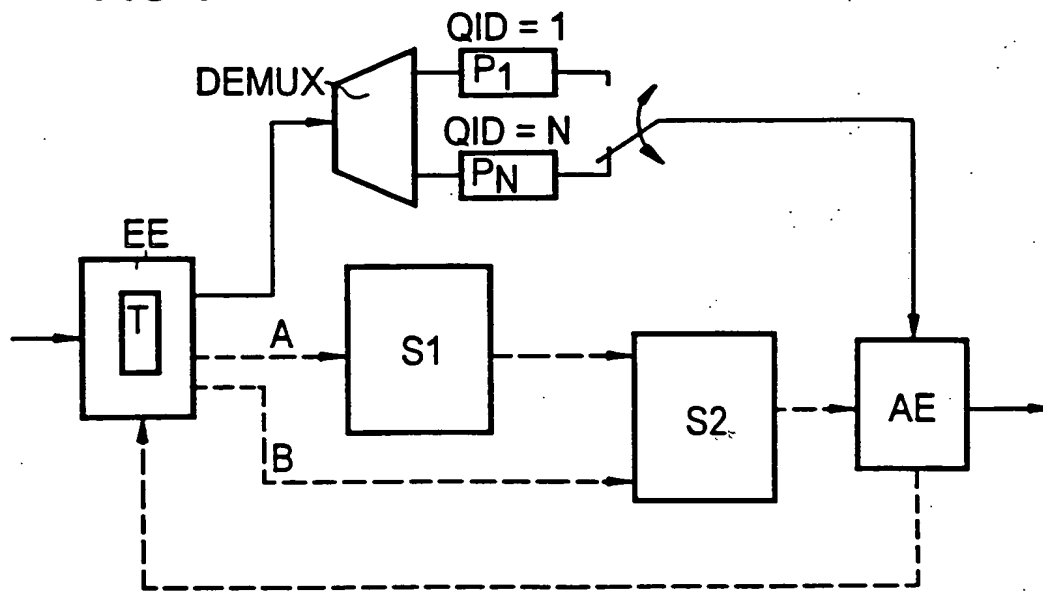
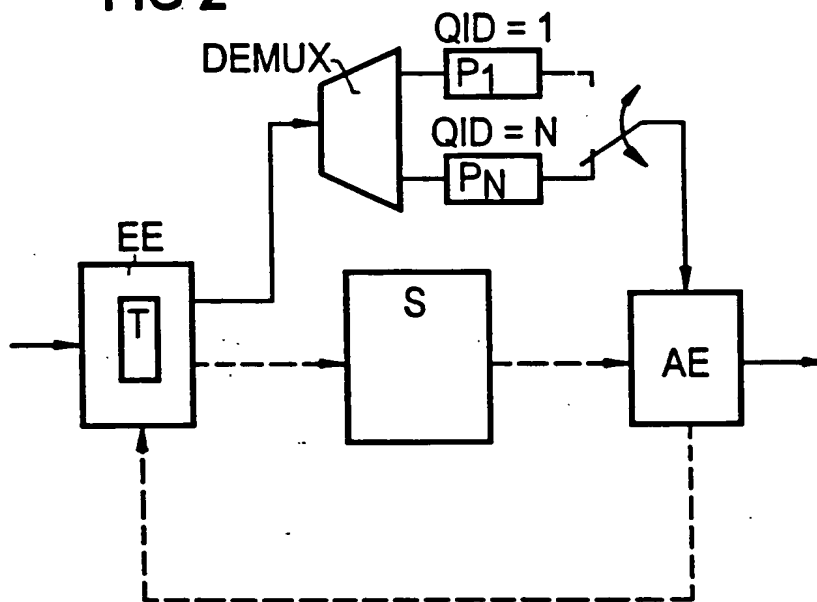


FIG 2



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The diagram shows a single input line entering a trapezoidal block labeled "DEMUX". From the right side of the block, multiple output lines emerge. Each output line passes through a rectangular buffer or delay element, represented by a rectangle divided into four smaller squares. The outputs are labeled r_1 , r_2 , and r_n at their respective terminals. A vertical ellipsis indicates intermediate outputs between r_2 and r_n . To the right of the demultiplexer outputs, there is a circular component labeled Q_S with a curved arrow indicating a feedback loop from its output back to its input.